Q.P. Code: 19EC4201 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester Regular Examinations Jan 2020

VLSI TECHNOLOGY

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Illustrate the main steps in a typical N-WELL process.	**8M**
	b	Explain the operation of CMOS inverter with a logic diagram.	**4M**
		OR	
2		Derive the relation between drain to source current I_{ds} VS drain to source voltage V_{ds} in non-saturated and saturated region.	**12M**

UNIT-II

3	**a**	Explain switch Logic and Alternative Logic.	**7M**
	b	Briefly discuss about the combinational logic functions.	**5M**
		OR	
4	**a**	Explain clearly the Scalable design rules.	**6M**
	b	Implement NAND gate in NMOS technology and hence draw its stick diagram and design a layout for the stick diagram.	**6M**

UNIT-III

5		What is simulation? Explain about various types of simulation applied at different levels of fabrication.	**12M**
		OR	
6	**a**	Discuss briefly about standard cell layout design.	**6M**
	b	Briefly explain the block diagram of phase locked loop for clock generation.	**6M**

UNIT-IV

7	**a**	Discuss about different floor planning tips.	**6M**
	b	Explain the concept of switch box routing.	**6M**
		OR	
8		Explain the concept of register transfer design with data path control architecture.	**12M**

UNIT-V

9	**a**	Write short notes on layout synthesis.	**6M**
	b	Discuss about global routing.	**6M**
		OR	
10		Explain about technology dependent logic optimization.	**12M**

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